Automated Synthesis Design Flow of Power Converter Circuits Aimed at SOC Applications

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Abstract—In this paper, we propose a power converter synthesis design flow aimed at SOC applications. A buck DC-DC converter and a low dropout (LDO) linear regulator, both with controllers are studied. We apply both the knowledge-based and the simulation-based methods in the proposed flow and they lead to an accurate result when it is compared with the design specification. Demonstration cases validate our work.

I- INTRODUCTION

Recent development of SOC integrates the digital and the analog/RF circuits, as well as the power processing circuit on a chip. The computer aid design tools for SOC have provided a complete and successfully support for the digital circuit design already. However, designers still need to adjust the analog and the RF circuit designs manually. Moreover, on chip power processing circuits to power different blocks of a SOC chip become a trend and their designs become very complicated [1]. Therefore, since the electronic industry is concerned about time to market, this may require the EDA tool to assist those designs.

TABLE I shows the comparisons of linear regulators and switching converters [2]. The buck converter can be applied to portable electronic products with high efficiency, like LCD-TVs, internet communication chips and cell phones. However, the inductor in the buck converter occupies a large area and it defeats the purpose of a SOC design. To reduce the size of switching converters, one can integrate the switches and the controller circuit in the SOC but leave the inductor and capacitors for off-chip connections. In the case of LDO, its efficiency is dominated by the input voltage and the output voltage difference, and thus the low drop out voltage is necessary.

To combine the advantages of both the switching converter and the LDO’s, one can connect a switching converter followed by a LDO to improve the fast transient response, such as a CPU load under a demand of intensive calculation [3]. An LDO alone can also be used for sensitive circuits, like audio amplifiers, analog and RF circuits. Because the buck converter and the LDO are often used as the power conversion units in SOC design, we select these two circuits as the test vehicle of automatic synthesis flows in this paper.

II- BUCK CONVERTER SYNTHESIS FLOW

Fig. 1 shows the buck converter circuit and Fig. 2 shows the buck converter synthesis flow. We use the closed form equations to calculate the design parameters. We also use the closed form equations to do the small signal analysis where the equations are the linearized equations unique to the switching power converter topology. Finally, we add HSpice to simulate the entire circuit to verify the design. As shown in Fig. 2, it starts with the input of specs listed as follows: the supply voltage ($V_s$), the output voltage ($V_o$), the max load current ($I_{o,max}$), the ripple current ($I_{rpp}$), the ripple voltage ($V_{rpp}$), the switching frequency ($f_s$) and the target efficiency. Next, steady state analysis is carried out to find the corresponding parameters of the buck converter in steady state operation, such as: the duty cycle ($D$), the inductance ($L$), the capacitance ($C$), and the width of the MOSs ($W_1$ & $W_2$) as switches. The small signal analysis is then carried out. The control circuit with a PID controller is also synthesized at this time and its small signal model is derived, the net-list is then generated before the final simulation of the entire circuit with HSpice.

Among these parameters, the current ripple and voltage ripple represent slight variations of inductor current and output capacitor voltage state variables during switching respectively [4], their functions are given by equations (1) and (2).

![Figure 1. Architecture of buck converter](image)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Linear Regulator</th>
<th>Switching Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Power Rating</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td>Size(PCB Real Estate)</td>
<td>Compact</td>
<td>Large</td>
</tr>
<tr>
<td>Cost and Complexity</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Noise</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

TABLE I. COMPARISONS OF DC-DC CONVERTERS
The required component values of the inductor and the capacitor are given by equations (3) (4). The converter efficiency is given by equation (5).

\[
\Delta I_L = I_L(T_s) - I_L(0) = \frac{V_o(1 - D)T_s}{L} \tag{1}
\]

\[
\Delta V = \frac{\Delta Q}{C} = \frac{1}{C} \frac{\Delta I_L}{2} = \frac{\Delta I_L}{28C_L} \tag{2}
\]

The power loss \( P_{\text{loss}} \) is given by equation (6).

\[
P_{\text{loss}} = 2P_{s1} + P_{s2} + P_{\text{ind}} + P_{\text{cap}} \tag{6}
\]

After the selection of the inductor and capacitor components from the vendors according to their spec., we include their series resistance for the efficiency calculation. Furthermore, the on-resistance of the MOS switch is also calculated. The equivalent circuit of buck converter of Fig. 3 is used for the efficiency calculation. \( r_p \) and \( r_n \) are the MOSs’ on-resistance, \( r_{dc} \) is the DC resistance of the inductor, and \( r_{esr} \) is the equivalent series resistance of the capacitor \( C \).

The transfer function of the PWM modulator \( G_p(s) \) is given by equation (9) where \( d(s) \) is the duty cycle, and \( v_e(s) \) is the error amplifier’s output voltage, both in the s-domain.

The Buck converter’s transfer function \( G_F(s) \) is given by equation (8) which consists of \( L \) and \( C \) mainly.

The whole circuit analysis with the controller [5] is shown in Fig. 4.

The open loop gain \( (G_{OL}(s)) \) is given by equation (7).

\[
G_{OL}(s) = G_F(s)G_p(s)G_{EA}(s) \tag{7}
\]

The Buck converter’s transfer function \( G_F(s) \) is given by equation (8) which consists of \( L \) and \( C \) mainly.

\[
G_F(s) = \frac{1}{s^2 + \frac{1}{LC}} \tag{8}
\]

The transfer function of the PWM modulator \( G_p(s) \) is given by equation (9) where \( d(s) \) is the duty cycle, and \( v_e(s) \) is the error amplifier’s output voltage, both in the s-domain.

\[
G_p(s) = \frac{d(s)}{v_e(s)} \tag{9}
\]

After we obtain all the coefficients needed and the small signal analysis using equations (1) to (9), the net-list of the design will be generated and the next step is to simulate the entire buck converter using HSpice. In an unusual situation, one might need to improve the specs. This is because the CMOS process technology used in this work might have some limitations like the allowable size and width selection of the MOSs and their corresponding switch on-resistance.

### III- LDO SYNTHESIS FLOW

Fig. 5 shows the circuit of LDO and Fig. 6 is the synthesis flow for LDO design. The small signal analysis is done with an equivalent circuit as shown in Fig. 7. Firstly, we require the user to key-in the process information and design specs, such as the process technology, the supply voltage \( (V_o) \), the output voltage \( (V_o) \), and the max load current \( (I_{L,max}) \). The synthesis flow generates the parameters of the sample resistance \( (R_{s1}, R_{s2}) \), the width of the power MOS \( (MP) \), the output capacitor \( (C_o) \), and the compensation series resistance \( (R_{esr}) \).
For LDO, we usually focus on the line regulation and the load regulation. Line regulation is given by equation (10). It is the ability to maintain a stable output voltage ($V_o$) under perturbation of input voltage ($V_i$). The load regulation is given by equation (11). It is the ability to maintain a stable output voltage ($V_o$) under load current ($I_L$) perturbation.

\[
\text{Line regulation} = \frac{\Delta V_o}{\Delta V_i}
\]

(10)

\[
\text{Load regulation} = \frac{\Delta V_o}{\Delta I_L}
\]

(11)

The controller of the LDO uses a feedback loop by comparing a reference voltage ($V_{ref}$) with the feedback voltage ($V_{fb}$), which is the partial voltage of $V_o$ given by equation (12).

\[
V_{fb} = \frac{R_{s2}}{R_{s1} + R_{s2}} V_o
\]

(12)

As for the efficiency, it is given by equation (13). The quiescent current is given by equation (14). $I_{qea}$ is the quiescent current of error amplifier (EA), $I_q$ is the quiescent current of the sample resistance.

\[
\text{efficiency} = \frac{I_L V_o}{(I_L + I_q) V_i} \times 100\% 
\]

(13)

\[
I_q = I_{qea} + I_{qs}
\]

(14)

In Fig. 7 of the small signal model of LDOs [6], $g_{ea}$ is the transconductance of the EA, $R_s$ is the output resistance of EA, $g_{mp}$ is the transconductance of power MOS (MP), $C_p$ is the gate-source capacitor of MP, and $R_{op}$ is the on-resistance of MP. The loop gain of the LDO consists of two poles ($P_{EA}$ and $P_{MP}$) and one zero ($Z_{out}$) which are given by equations (15) (16) and (17).

\[
P_{EA} = \frac{1}{2\pi R_c P C_p}
\]

(15)

\[
P_{MP} = \frac{1}{2\pi R_{op} C_o}
\]

(16)

\[
Z_{out} = \frac{1}{2\pi R_{csr} C_o}
\]

(17)

In an unusual case, if the system is unstable, we can change the value of $Z_{out}$ by fixing the value of $R_{csr}$ and add a resistance ($R_{add}$) in series with it as given by equation (18).

\[
R_{csr} = R_{esr} + R_{add}
\]

(18)

IV- AUTOMATION SELECTION FLOW

This paper does not only automate the design of power converters but it also optimizes the design by selecting the most suitable architecture according to the specifications and the foundry process corners.

At first, the user keys-in the input voltage ($V_i$), the output voltage ($V_o$), the maximum output current ($I_{L,max}$), and the efficiency ($\eta$) as before, then the tool generates the steady-state design parameters and it carries out the small signal analysis for both the buck converter and the LDO respectively with different process corners. The flow automatically selects a suitable architecture according to the highest efficiency that is set by the user. Third, it provides the proposed architecture. However, if there is a determined architecture, the flow still can complete the design after the user selects it directly.

V- DESIGN EXAMPLES

We use a few demo cases to verify the correctness of our work. TABLE II shows two demo cases and the results of the buck converter with the process technology of TSMC 0.18μm 3.3volt. TABLE III shows the output design parameters of two test cases. TABLE IV shows different corner case results of buck converter when MOSFET at FF (fast-fast or best) and SS (slow-slow, or worst). TABLE V shows the performance of the buck converter with the inductor tolerance of ±10%. Fig. 8–9 shows the simulated output voltage ripples of case 1 and 2. They are within the specs.
TABLE II. DEMO CASES OF BUCK CONVERTER

<table>
<thead>
<tr>
<th>Item</th>
<th>Case1</th>
<th>Case2</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{in} (V)</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>I_{L,max} (mA)</td>
<td>359</td>
<td>359</td>
</tr>
<tr>
<td>P_s (mW)</td>
<td>718.3</td>
<td>718.3</td>
</tr>
<tr>
<td>V_{out} (mV)</td>
<td>33.3</td>
<td>≤ 24</td>
</tr>
<tr>
<td>η (%)</td>
<td>≥ 80</td>
<td>80.6</td>
</tr>
</tbody>
</table>

For the LDO, we also use two demo cases and results are shown in TABLE VI. TABLE VII shows the output design parameters of two test cases. Simulation results show the line to output and load to output regulations. TABLE VIII shows synthesis results of LDO with MOSFET Spice parameters at FF (best) and SS (worst) cases. They are within the specs.

VI- CONCLUSION

Automated synthesis design flow of power converter blocks aimed at SOC application is proposed. The design flow consists of the equation-based and the simulation-based methods. A DC-DC buck converter and a LDO designs are demonstrated with the proposed flow. We include the parasitic resistance of both the passive and active devices in the design to analyze the power conversion efficiency. This work also includes the controller designs to regulator the output voltage of the converters. Demonstration cases show that the designs meet the specs. However, we need a real silicon verification to verify our work which is the limitation of this paper. In the future, we will focus on the optimization of synthesis flow and include more power converter architectures and more controller options to generate on chip power converter designs for multiple-voltage SOC applications.

REFERENCES


