A Low Power Compact Size Forward Body-Biased K-Band CMOS Low Noise Amplifier

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Abstract — This paper developed a forward body-bias technique to reduce the power consumption of a low power and compact size low noise amplifier (LNA) in tsmc™ 0.18 μm CMOS technology. The LNA can operate at very low power consumption of 4.9 mW from a 0.7-V supply voltage. The proposed LNA achieves a gain of 11 dB and an input IP3 of -7.5 dBm at 25 GHz. The operating bandwidth is from 24 to 26.5 GHz. The chip is very compact of the size of 0.71 mm by 0.56 mm.

Index Terms — CMOS, forward body-biased technique, LNA, mm-wave.

I. INTRODUCTION

Recently, there are many interesting evolutions in high-data-rate short range radar products which can be implemented in radio frequency system-in-a-chip (RF-SoC) techniques. Since the accuracy of range resolution has to be a few centimeters, high frequency bands such as millimeter wave are chosen as carrier frequency to realize the RF front. In the past, some exotic technologies, such as GaAs pHEMT, and mHEMT, have been dominated in mm-wave integrated circuit designs. Thanks to continuous down-sizing in CMOS technology, CMOS has become an alternative candidate at mm-wave frequency range. CMOS technology has more mature process capability and provides the advantages of low-cost silicon wafer, high-level integration, good thermal conductivity, and excellent chip integration [1]. However, some challenges still need to overcome in mm-wave CMOS IC design, such as the frequency limits of active devices, the poor isolation of signals from low-resistivity silicon substrate, and high power consumption. The goal of this work is to design a K-band LNA with low power consumption at low supply voltage and compact chip size in standard tsmc™ 0.18 μm CMOS technology. The proposed forward body-bias technique is adopted to optimize the minimal power consumption at very low supply voltage of 0.7 V.

II. LOW NOISE AMPLIFIER DESIGN

Figure 1 shows the schematic diagram and its detail design parameters of the single-ended LNA with a three-stage common-source configuration. The common-source topology is usually implemented in mm-wave circuit to reduce the power consumption and noise figure (NF). The source degeneration scheme in each stage is used to match 50 Ω of the input impedance while these inductors resonate out the gate-source capacitors (Cgs). Another advantage of this scheme is that the optimal impedances of the input return loss and NF at the desired frequency can be taken closer together by selecting appropriate degeneration inductor and gate inductor. These inductors can be realized by either transmission line or lumped inductor [2], [3]. The lumped inductor approach possesses smaller chip area but is susceptible to more substrate coupling which also makes larger discrepancies between the simulation and measurement. Therefore, it needs more EM simulation iterations and results in a long design cycle. On the other hand, transmission line inductor gains faster design cycles with more precise inductor value than that used by lumped inductor. The quality factor of transmission line inductor is more than 10 which is better than its lumped element counterpart. Moreover, the layout of the transmission line inductor can be arranged in meandered form. These meandered-line inductors usually have more compact area than those inductors provided by foundry’s process design kit (PDK). In this design, all inductors (L1~L13) are implemented by meandered-line inductor to achieve small chip size.

The forward body-bias technique is applied to reduce the threshold voltage \(V_{th}\). The use of the forward body-bias technique has been developed in low power consumption mixer and LNA designs which operation frequencies are from 2.4 to 6.5 GHz [4]-[7]. This work shows the feasibility of this technique in a K-band LNA design. The threshold voltage of MOS transistor is modeled in below,

\[
V_{th} = V_{th0} + \gamma \sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}
\]

where \(V_{th0}\) is the threshold voltage at \(V_{BS}=0\); \(\gamma\) is the body effect coefficient; \(\phi_f\) is the bulk Fermi potential; \(V_{BS}\) is the voltage between body and source terminal. Thus, \(V_{th}\) can be varied by changing the \(V_{BS}\) that a dynamic threshold voltage of MOS transistor can be obtained.
Friis’s formula is useful to evaluate the total noise performance of the multistage design. The relation of the total noise factor for cascade scheme can be given as,

$$NF_{\text{total}} = NF_1 + \frac{NF_2 - 1}{A_{R_1}} + \frac{NF_3 - 1}{A_{R_1} \times A_{R_2}} + \frac{NF_4 - 1}{A_{R_1} \times A_{R_2} \times A_{R_3}} + \cdots \tag{2}$$

where the $NF_n$ and $A_{R_n}$ are the noise factor and available gain of the $n$-stage amplifier, respectively. According to (2), the total NF is mainly contributed from the first stage in the cascade amplifier. In order to reduce the power consumption and supply voltage of the first stage, Fig. 2 shows the simulated bias conditions ($V_{dd}$ and $V_{b2}$) against the power consumption. Assuming all transistors operate in saturation region ($V_{gs} \geq 0.2 \, \text{V}$), while the suitable current density of the minimum NF has been designed by a value of 0.049 mA/\mu m. Various biasing conditions are simulated to achieve the lowest power consumption of the first stage. The gate bias $V_{g1}$ is set to 0.55 V. As indicated in Fig. 2, the optimal biasing conditions for the lower power consumption in the first stage LNA are the supply voltage $V_{dd} = 0.7 \, \text{V}$, and body bias $V_{b2} = 0.4 \, \text{V}$, respectively. Thus, the power consumption of the first stage can be reduced by using the forward body-bias technique. In this design, the bias current for the first stage is 2.2 mA. The second stage is designed for high small-signal gain that is biased at 2.4 mA. The third stage is designed to not only provide extra small-signal gain but also to match the output matching for measurement requirement. The bias current of the third stage is 2.4 mA. The total power consumption is 4.9 mW at 0.7 V supply voltage. The total width (W) is calculated as 45 \mu m for each stage under the fixed power consumption of 4.9 mW. Figure 3 shows the simulations of the NF and maximal available gain (MAG) in the combinations of the number of finger (N) and width (W) at total width of 45 \mu m of the MOS transistor that are used to trade-off the performance between NF and MAG. The transistor size is chosen by 3×15 \mu m to have the minimal NF of 1.75 dB with an moderate MAG of 7.3 dB. The optimum device size selection together with forward body-bias technique allows the LNA to operate at very low supply voltage of 0.7 V, and meanwhile maintains good performance of gain and NF. The matching is performed with a source-degenerate inductor design procedure. All inductors as shown in Fig. 1 are replaced by transmission line inductors to implement the matching network. The 3D EM simulator ADS MOMENTUM™ was used to simulate every transmission line inductor and interconnection in the layout. The large...
bypass capacitors $C_{\text{bypass}}$ and resistor $R_{\text{bypass}}$ are used to eliminate from parasitic effects which may induce noise from DC power supply. Both $C_{\text{in}}$ and $C_{\text{out}}$ are the DC blocking capacitors to block the DC level.

III. MEASUREMENT RESULTS

Figure 4 shows the chip microphotograph of the designed single-ended LNA using the forward body-bias technique. The die area including test pads and dummy blocks is 0.71 mm by 0.56 mm. The performance of the LNA was measured by using Agilent™ 67 GHz Vector Network Analyzer (VNA) and Cascade probe station with on-wafer GHz probes. The LNA is biased at a 0.7-V supply voltage with total current of 7 mA. The total DC power consumption is 4.9 mW. To the best knowledge of the authors, this may be the lowest power consumption for K-band CMOS LNAs. The S-parameters of the designed single-ended LNA are simulated by Agilent ADS™ and its EM simulator. As shown in Fig. 5, the designed single-ended LNA has a gain of 11 dB at 25 GHz with a 1-dB bandwidth of 2.5 GHz from 24 to 26.5 GHz. The peak $S_{21}$ has only 0.1 dB discrepancy between the measurement and simulation at the same bias condition. The input and output return losses are shown in the Fig. 5. Both the input and output return losses are better than 6 dB. The isolation is better than -30 dB across the full bandwidth.

Figure 6 shows the output power and linearity performance. The input-referred 1-dB compression point is -16 dBm and the input third intercept point is -7.5 dBm at 25 GHz. Figure 7 shows the simulated and measured NF against the frequencies. The measured NF is from 5.12 dB to 5.31 dB within the operating frequency bandwidth.

The figure of merit (FoM) concerning gain, noise factor and power consumption of LNA is defined for fair comparison [8]. The FoM as given in (4) is the ratio of the gain in dB and bandwidth in GHz to the product of noise factor minus one, DC power consumption in mW, and chip area in mm².
Table I summarizes the performance of the single-ended LNA and benchmarks previously reported LNAs operating above 20 GHz. As can be seen, this work achieves the minimum power consumption with a small supply voltage, compact chip size, reasonable power gain, NF and linearity as compared with other CMOS LNA designs. The designed single-ended LNA has the FoM of 5.34 which is the highest one among all cited references.

![Table I. Comparison of Previously Reported LNAs Operating above 20 GHz.](image)

*excluding the pads and buffer

### IV. CONCLUSION

A 25 GHz single-ended CMOS LNA has been demonstrated by using the forward body-bias technique to achieve low power consumption at a very low supply voltage of 0.7 V. The designed LNA has a gain of 11 dB and an input IP3 of −7.5 dBm at 4.9 mW power consumption. The chip is very compact of the size of only 0.4 mm². Based on these measurement results of the designed LNA, it is shown that the common-source topology yields both good NF and compact size for high frequency LNA design.

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