Linearity Enhancement of CMOS Device using a Modified Third-Order Transconductance Cancellation Technique for Microwave Amplifier

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Abstract — This paper presents linearity enhancement of CMOS device for microwave amplifier applications. The proposed method is based on a modified third-order transconductance (gm3) cancellation technique and the device is fabricated in 0.13 μm CMOS process. For the NMOS device with the proposed gm3 cancellation technique, the third-order intermodulation distortion (IMD3) is improved by 15 dB as compared to the conventional single device. Two Ka-band CMOS amplifiers with and without the linearization are successfully evaluated. With the linearization, the measured IMD3 is enhanced by 14 dB, and the adjacent channel power ratio (ACPR) of the amplifier is improved by 7 dB for a 64-QAM modulation signal. Moreover, the linearization scheme is easily applied to the microwave amplifier and mixer designs without extra dc power consumption.

Index Terms — Amplifier, CMOS, linearization, third-order transconductance.

I. INTRODUCTION

Linearity of radio frequency (RF) amplifiers is critical specification in digital modulation systems, especially for the modern communication applications [1]. The linearity can be enhanced using pre-distortion techniques based on digital [1] or analogy circuit [2]. Nevertheless, the reported methods have some limitations for monolithic microwave integrated circuits (MMICs), such as modulation bandwidth, complexity, and dc power consumption. The advanced development of CMOS technology has shown that the CMOS devices have potential for the millimeter-wave (MMW) applications [3]. For the linearization of the CMOS circuits, a diode connected MOSFET as a predistorter was proposed to improve the linearity of a cascade power amplifier [4], and multiple-gated transistor (MGTR) linearization schemes were reported in [5] and [6] for a RF amplifier and a Gilbert cell mixer, respectively. A capacitance desensitization technique was proposed to reduce third-order intermodulation distortion (IMD3) of a MGTR amplifier [7]. However, most of them are below than 10 GHz. In the MMW bands, a linearizer was implemented using a shunt cold-mode high-electron mobility transistor (HEMT) for a 44-GHz power amplifier [8]. A W-band high-power direct-conversion transmitter was improved using a digital predistortion technique [9].

In this paper, the proposed linearization for the CMOS device is based on a third-order transconductance (gm3) cancellation technique [10] which is adopted two parallel transistors with negative and positive gm3 to get a flat gm3 region. Owing to the nonlinearity of the device, the transconductance can be expressed as a power series that contains n kinds of the n-th-order transconductance. The IMD3 of the device is usually dominated by the gm3 [11]. Therefore, the linearity of the amplifier can be improved by reducing the gm3 of the MOSFET. In order to achieve good linearity with high dynamic range, we use three parallel transistors with proper values of gm3 for the linearization. The equivalent device cell has a flat gm3 region with wide gate bias range, and also the IMD3 of the device cell is improved by 15 dB. The proposed method can be easily implemented without additional dc power consumption and other complex circuit. Moreover, two Ka-band CMOS amplifiers with and without the linearization are successfully fabricated in a commercial 0.13 μm CMOS process. With the linearization, the measured IMD3 of the amplifier is enhanced by 12 dB. The two Ka-band CMOS amplifiers also have been evaluated using high-speed wideband digital modulation signals. The amplifier with the linearization features good modulation quality and adjacent channel power ratio (ACPR). The modified gm3 cancellation technique shows wide dynamic range with good linearity as compared to the conventional cancellation technique, and can be further applied to the microwave and MMW transceivers due to its linearity improvement and design methodology.

II. DEVICE CELL AND CIRCUIT DESIGN

The proposed linearization concept is realized using a TSMC commercial standard bulk 0.13 μm CMOS process. The NMOS device exhibits a unity current gain frequency (fT) of 90 GHz and a maximum oscillation frequency (fmax) of 100 GHz with a dc supply voltage of 1.2 V. The transconductance of the NMOS device can be expressed as

\[ g_m = \mu_n C_{OX} W / L \left[ V_{gs} - V_T \right] \]

\[ V_T = V_{T0} + \gamma \sqrt{2\phi_F - V_{bs}} - \gamma \sqrt{2\phi_F}, \]

where \( \mu_n \) is the electron mobility, C_{OX} is the oxide capacitance, \( W \) is the device width, \( L \) is the channel length, \( V_{T0} \) is the zero substrate bias threshold voltage, \( \phi_F \) is the surface potential, \( V_{bs} \) is the voltage between the bulk and source, and \( \gamma \) is the body effect factor. The transconductance is a function of the voltage \( V_{bs} \), as well as the \( g_{m3} \). The characteristic of the \( g_{m3} \) can be adjusted by varying the body bias. Furthermore, the \( g_{m3} \) will be reduced if the transistor is
connected to the other transistor with proper body bias. The equivalent schematics of 1, 2 and 3 parallel transistors and the simulated $g_{m3}$ of the three device cells are shown in Fig. 1, where M3, M4, and M5 have total gate widths of 2.5×10, 2×20, 2×16 and 2×30 μm, respectively. The gate biases are all 0.5 V, and the body biases of $V_{b1}$ and $V_{b2}$ are -1.1 and -2.6 V, respectively. The simulated $g_{m3}$ for the case of $n=3$ demonstrates a flat $g_{m3}$ region with wide gate bias range from 0.5 to 0.7 V. Based on a two-tone simulation, the IMD3 of the 3-parallel device cell is improved by 15 dB as compared to the single-device cell.

![Schematics of 1-, 2- and 3-parallel transistors](image1)

![Simulated $g_{m3}$](image2)

Fig. 1. (a) Equivalent schematics of 1-, 2- and 3-parallel transistors, and (b) the simulated $g_{m3}$ of the three device cells versus $V_{gs}$.

The 3-parallel device cell is further applied to the microwave amplifier design. The schematics of the two Ka-band CMOS amplifiers with and without the linearization of the $g_{m3}$ cancellation are shown in Fig. 2. The amplifiers consist of three common-source (CS) stages. For the amplifier with the linearization, the $g_{m3}$ cancellation is only applied to the output stage due to the design considerations of the linearity and the small signal gain. In general, the output stage of the amplifier more suffers from the nonlinearity of the transistor since the output power of the output stage is higher than the input and drive stages. The gate widths of the NMOS M1, M2, and M3 in the first, second and output stages are all 2 μm with 20 fingers. The input and output matches of the amplifiers are both adopted an one-section inductance-capacitance (LC) network, and the inter-stage matches between the first, the drive and the output stages are all based on a conjugate matching network. In order to enhance the stability of the amplifiers, all the CS stages are designed with source degenerative inductors L7, L8 and L9. On-chip bypass capacitors (C1, C2, C3, C8, C9 and C10) are used for in-band RF bypass. The inductors L1 ~ L6 are all designed using the coplanar waveguide (CPW) structure to further reduce the metal loss.

The passive components, including the inductors, capacitors, and transmission lines, are all simulated with a full-wave electromagnetic (EM) simulator [12]. The dc power consumptions of the two amplifiers are both 5 mW with a dc supply $V_{DD}$ of 1.2 V. The chip photos of the K-band CMOS amplifiers with and without linearization are shown in Fig. 3. The chip sizes are both 0.75 × 0.65 mm², including RF and dc bias PADs.

![Schematics of the Ka-band CMOS amplifiers](image3)

![Chip photos of the Ka-band CMOS amplifiers](image4)

Fig. 2. Schematics of the Ka-band CMOS amplifiers, (a) with linearization and (b) without linearization.

Fig. 3. Chip photos of the Ka-band CMOS amplifiers, (a) with linearization and (b) without linearization. The chip sizes are both 0.75 × 0.65 mm², including RF and dc bias PADs.
III. EXPERIMENTAL RESULTS AND DISCUSSIONS

To verify the third-order nonlinear characteristic of the amplifiers with and without the linearization, the two-tone intermodulation power sweeps are measured with a frequency spacing of 1 MHz. At 28 GHz, the measured IMD3 improvement between the two amplifiers with and without linearization is plotted in Fig. 6. As $V_G$ is 0.6 V, the measured IMD3 of the amplifier with the linearization is enhanced by 14 dB. The measured output third-order intercept point (OIP3) is also improved by 5 dB from 9 to 14 dBm. The measured noise figures of the two amplifiers are both 4.5 dB. The linearity of the amplifier is highly enhanced without degrading the noise figure performance.

Furthermore, to verify whether the linearization is suitable for the modern communication systems, a high-level modulation scheme 64-QAM modulation signal with a data rate of 1 Mbps and an orthogonal frequency division multiplexing (OFDM) modulation signal with a data rate of 54 Mbps are adopted for the evaluation. The measured output spectrums of the 64-QAM and OFDM modulation signals with and without the linearization are plotted in Fig. 7 (a) and (b), respectively. For the 64-QAM modulation signal, the measured ACPR is improved by 5 dB for both first and second offset channels. For the OFDM modulation signal, the measured ACPR is improved by 4 dB for first offset channel. Due to the spectrum spread, the output spectrum of the second channel is lower than the noise floor of the measured system.

The measured OFDM 64-QAM constellation diagrams with and without the linearization are plotted in Fig. 8 (a) and (b), respectively. For the measured modulation quality, the measured error vector magnitude (EVM) is enhanced by 6 dB from -27 to -33 dBc, and the measured recovery symbols converge on 64 reference constellations for the amplifier with the linearization. From the experimental results, we can see that the linearity of the CMOS amplifier can be highly improved by using the modified $g_m$ cancellation technique in MMW bands without extra dc power consumption. The concept of the modified $g_m$ cancellation technique is also suitable for the MMW circuits.
IV. CONCLUSION

In this paper, a linearization scheme of the modified $g_{m3}$ cancellation is adopted to improve the linearity of the CMOS device. Two Ka-band CMOS amplifiers with and without the linearization are successfully evaluated using a 0.13 μm CMOS process. Without extra dc power consumption and complex circuit, the linearity of the amplifier is further improved by the linearization method. The linearization technique is suitable for the microwave and MMW CMOS active circuits, especially for the high speed digital communication systems with high-level modulation scheme, due to the linearity improvement of the device and the low dc power consumption.

![Fig. 7. Measured two-tone intermodulation power sweep of the proposed amplifier with and without the linearization.](image)

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Fig. 8. Measured 64-QAM OFDM constellation diagrams of the two amplifiers (a) with the linearization, and (b) without the linearization.

REFERENCES